DESIGN NOTES

LTC1564: A Digitally Tuned Antialiasing/Reconstruction Filter Simplifies High Performance DSP Design – Design Note 276

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Introduction

Typically an analog antialiasing filter is used to band-limit wideband signals at the input of an analog-to-digital converter. In addition, as the converter's sampling rate changes, an antialiasing filter's passband should increase or decrease accordingly. A frequency-tunable analog filter for a high resolution converter requires a large number of expensive precision components. With the LTC®1564, designers of data acquisition instruments and digital signal processing (DSP) systems have a low noise, continuous-time, "brick wall" lowpass filter with digital control of the corner frequency f_C, (f_C range 10kHz to 150kHz in 10kHz steps). The LTC1564 also includes a digitally programmable gain amplifier (PGA, 1V/V to 16V/V in 1V/V steps). A simple, on-chip, latching digital interface controls corner frequency and gain settings. The LTC1564 is in a small 16-pin SSOP and operates from a supply voltage of 2.7V to 10.5V total (single or split supplies).

Filtering Performance and Operation

The LTC1564 is a high resolution filter with a rail-to-rail output. The 8th order lowpass response with two stopband notches gives approximately 100dB attenuation at 2.5 times f_C, making it suitable for high resolution antialiasing filtering. Despite the high filter order, the wideband noise is only 33µV_{RMS} (typical) at a 20kHz corner frequency and unity gain, which is 100dB below the rail-to-rail maximum signal level for ±5V supplies. The output-referred noise rises only slightly at higher gain settings. At the maximum 24dB (16V/V) gain setting, the same 20kHz response just quoted has an output noise level of 40µV_{RMS} (or an input-referred noise of 2.5µV_{RMS}). Gain control in the LTC1564 is an integral part of the filter, using a proprietary method that deliberately minimizes the total noise. This feature is very difficult to achieve with separate variable gain amplifiers and filter circuits. The LTC1564 satisfies a demand for lowpass filters with roughly "100-100-100" performance: 100dB stopband attenuation, 100dB signal-to-noise ratio (SNR) and 100kHz bandwidth.

You do not have to be a filter expert or analog designer to use the LTC1564. There are only three analog pins: Input, Output and a half-supply reference voltage point, AGND (Figure 1). The other pins are digital controls and power supply. The LTC1564 is an instrument in a box with analog input and output jacks and two rotary switches labeled "Frequency" and "Gain." The frequency setting "F" and gain setting "G" are 4-bit codes entered through the F and G digital input pins (Table 1). In addition, setting the F code to 0000 engages a "mute" state where the filter remains fully powered but the gain is a hard zero (typically –100dB). Logic levels for the LTC1564 digital inputs are nominally rail-to-rail CMOS (where a logic 1 is V^+ and a logic 0 is 0V for single 3V or 5V or dual ±5V supply operation).

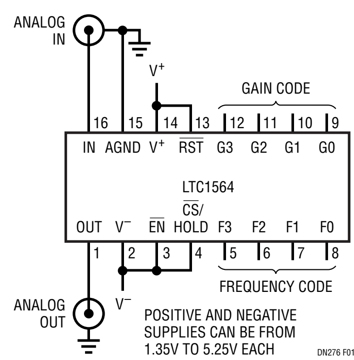

Figure 1. Dual Power Supply Circuit

Table 1. Programming the Corner Frequency and Gain of the LTC1564

F3	F2	F1	F0	G3	G2	G1	G0	MODE
0	0	0	1	0	0	0	0	f_C = 10kHz, Passband Gain = 1V/V (0dB)
1	1	1	1	0	0	0	0	f_C = 150kHz, Passband Gain = 1V/V (0dB)
0	0	0	1	1	1	1	1	f_C = 10kHz, Passband Gain = 16V/V (24dB)
0	0	0	0	Don't Care				Mute State, Zero Gain

Application Example: 2-Chip "Universal" DSP Front End

In Figure 2, an LTC1564 filter drives an LTC1608 16-bit 500ksps analog-to-digital converter (ADC) for a highly flexible, complete 16-bit analog-to-digital signal interface with variable gain, variable sampling rate and variable analog bandwidth up to 150kHz. The LTC1564's frequency-setting "F" code and the rate of sampling controlled by the LTC1608's CONVST input (Pin 31) set signal bandwidth and antialiasing filtering.

As an example, with the LTC1564 passband corner (f_C) set to 100kHz, with a sampling rate (f_S) of 500ksps by the LTC1608 ADC, provides 100dB of antialiasing protection at the critical analog folding frequency of $f_S/2$, or 250kHz. Another independent option is to sample at a rate (f_S) that is lower than $5 \bullet f_C$. This will move the folding frequency ($f_S/2$) down from $2.5 \bullet f_C$ to somewhere within the analog filter's roll-off band, where the filter's rejection will not be as high as 100dB. This reduces the antialias rejection for signals at and above $f_S/2$, but still provides sufficient antialias protection in many applications, particularly if, as is often true, the aliasable signals at and above $f_S/2$ have lower levels than the desired signals at and below f_C. The circuit of Figure 2 can accommodate either or both of these options by suitable choice of ADC sampling rate and filter F code.

Figure 3 shows a measured FFT spectrum of the digital output of Figure 2's circuit. A 40kHz, $100mV_{RMS}$ sine wave was preamplified to $4.5V_{P-P}$ by the LTC1564 to nearly span the input range of the LTC1608 ADC. The LTC1564 is set for a cutoff frequency of 50kHz and a gain of 16V/V and the sampling frequency of the ADC is 204.8kHz. Total harmonic distortion (THD) is 86dB down and the dynamic range is 109dB (since the filter noise does not increase with gain, the programmable filter gain extends the dynamic range beyond the unity gain range).

Conclusion

In addition to providing high resolution antialiasing, the LTC1564 is useful as a reconstruction filter that eliminates the nonessential high frequency signal spectrum at the output of a digital-to-analog converter (DAC). A simple, compact, economical and high performance digital signal processing and generating system hardware requires only two LTC1564, an ADC and a DAC.

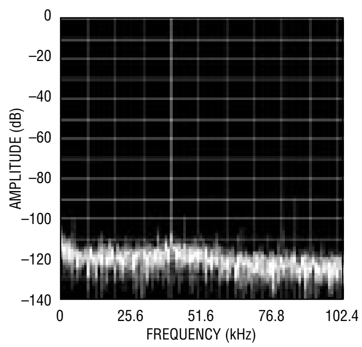

Figure 3. FFT Plot of the Digital Output of Figure 2's Circuit

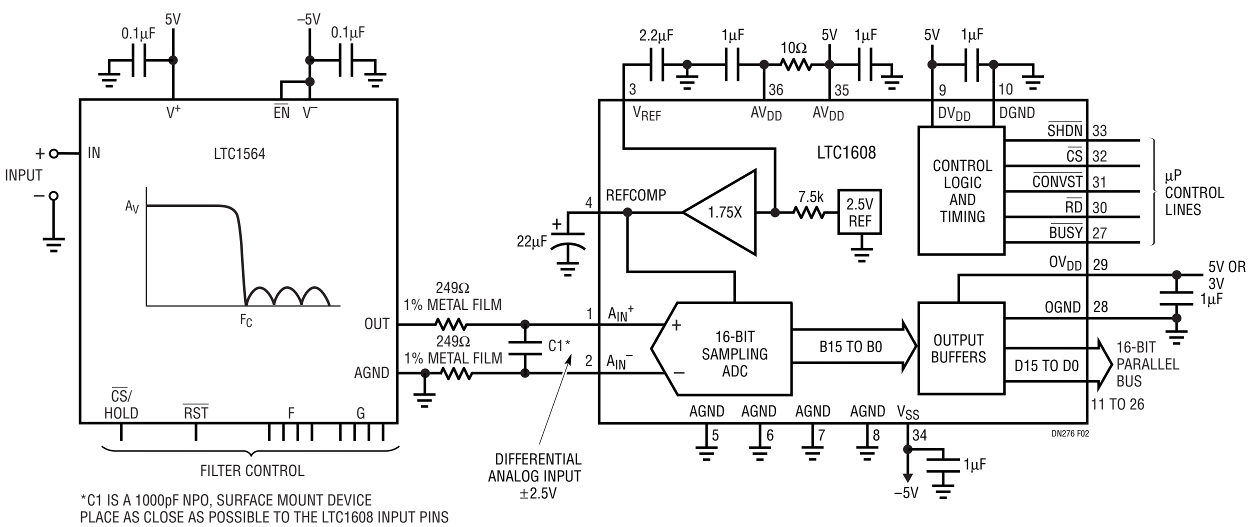

Figure 2. A Universal DSP Front End

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